AMENDMENTS TO THE CLAIMS:

Complete Listing of Claims

Claim 1. (previously presented) A microcontroller integrated circuit (IC) comprising:

a program memory for storing a program to be executed;

a program counter coupled to the program memory for selecting address locations in said memory;

a program counter copy register for storing a program memory address pointed to by said program counter as a return address from a debug monitor routine;

instruction execution circuitry coupled to the program memory for executing instructions received from said memory;

a breakpoint address register for storing a breakpoint address;

address compare circuitry for comparing a value in said program counter to a value in said breakpoint address register, said compare circuitry providing a breakpoint signal upon detection of a valid breakpoint address comparison; and

a multiplexer interposed between said program memory and said program execution circuitry, said multiplexer comprising circuitry for inserting a debug instruction into the instruction execution circuitry upon receipt of said breakpoint signal, wherein said debug instruction is substituted for an instruction in a program memory address pointed to by said program counter.

Claim 2. (original) The microcontroller IC of claim 1, further comprising:

a stack pointer register;

a stack breakpoint register for storing a stack trap address;

stack pointer compare circuitry for comparing a value in said stack pointer register to a value in said stack breakpoint register, said stack pointer compare circuitry providing a stack trap signal upon detection of a valid stack pointer address comparison; and

wherein said multiplexer inserts said debug instruction into the instruction execution circuitry upon receipt of said stack trap signal.

Claim 3. (original) The microcontroller IC of claim 2, wherein said valid stack pointer address comparison is selected from the group consisting of: said value in said stack pointer register being equal to said value in said stack breakpoint register, said value in said stack pointer register being greater than said value in said stack breakpoint register, said value in said stack pointer register being less than said value in said stack breakpoint register, and combinations thereof.

Claim 4. (original) The microcontroller IC of claim 1, further comprising single step circuitry directing said multiplexer circuitry to insert said debug instruction into the instruction execution circuitry after the execution of each instruction of an application program.

Claim 5. (original) The microcontroller IC of claim 1, wherein said debug instruction is a long jump instruction to a debug monitor routine.

Claim 6 (canceled)

Claim 7. (original) The microcontroller IC of claim 1, wherein said address comparison circuitry further comprises memory bank comparison circuitry for detecting a specific bank access in addition to said breakpoint address.

Claim 8. (previously presented) An embedded microcontroller apparatus comprising:

a circuit board embedded in the apparatus;

a microcontroller integrated circuit disposed on said circuit board, including

a program memory for storing a program to be executed,

a program counter coupled to the program memory for selecting address locations in said memory,

a program counter copy register for storing a program memory address pointed to by said program counter as a return address from a debug monitor routine, and

debug circuitry disposed on said microcontroller integrated circuit, said debug circuitry comprising

compare circuitry for comparing a breakpoint address to instruction fetch addresses in said program memory, said compare circuitry generating a breakpoint signal indicating a valid address compare; and

multiplexer circuitry coupled to said compare circuitry, said multiplexer circuitry, upon receiving said breakpoint signal, substituting a debug program instruction for execution by the microcontroller in place of a standard instruction fetched from program memory.

Claim 9. (original) The embedded microcontroller apparatus of claim 8, wherein said apparatus is a universal serial bus controller.

Claim 10. (original) The embedded microcontroller apparatus of claim 8, wherein said microcontroller further comprises a stack pointer register, and said debug circuitry further comprises:

a stack breakpoint register for storing a stack trap address; and

stack pointer compare circuitry for comparing a value in said stack pointer register to a value in said stack breakpoint register, said stack pointer compare circuitry providing a stack trap signal upon detection of a valid stack pointer address comparison; wherein said multiplexer substitutes said debug program instruction for execution by said microcontroller upon receiving said stack trap signal.

Claim 11. (original) The embedded microcontroller apparatus of claim 10, wherein said valid stack pointer address comparison is selected from the group consisting of: said value in said stack pointer register being equal to said value in said stack breakpoint register, said value in said stack pointer register being greater than said value in said stack breakpoint register, said value in said stack pointer register being less than said value in said stack breakpoint register, and combinations thereof.

Claim 12. (original) The embedded microcontroller apparatus of claim 8, said debug circuitry further comprising single step circuitry directing said multiplexer circuitry to substitute said debug program instruction for execution by said microcontroller after the execution of each standard instruction fetched from program memory.

Claim 13. (original) The embedded microcontroller apparatus of claim 8, wherein said debug program instruction is a long jump instruction to a debug monitor routine.

Claim 14 (canceled)

Claim 15. (previously presented) A method of debugging a microcontroller integrated circuit, said method comprising:

storing a breakpoint address in a hardware register on said microcontroller integrated circuit;

executing an application program from program memory by said microcontroller;

comparing application program instruction addresses to said breakpoint address;

halting execution of said application program upon detection of an instruction fetch from a memory address equal to said breakpoint address;

storing said memory address in a program counter copy register, wherein said address is reloaded into said program counter after execution of said debug routine;

substituting a jump instruction to a debug program for said instruction fetched from said memory address; and

executing said debug program.

Claim 16. (original) The method of claim 15, further comprising:

storing a stack trap address in a stack breakpoint hardware register on said microcontroller;

comparing stack pointer addresses to said stack breakpoint address; and

upon detection of a valid stack pointer address comparison, performing said halting execution, said substituting said jump instruction, and said executing said debug program steps.

Claim 17. (original) The method of claim 16, wherein said valid stack pointer address comparison is selected from the group consisting of: said stack pointer address being equal to said stack breakpoint address, said stack pointer address being greater than said stack breakpoint address, said stack pointer address being less than said stack breakpoint address, and combinations thereof.

Claim 18. (original) The method of claim 15, said executing said debug program comprising:

providing status information to external circuitry; and

receiving new breakpoint address information.

Claim 19 (canceled)

Claim 20. (previously presented) The method of claim 15, further comprising pushing the address stored in the program counter copy register onto a stack and executing a return to said application program at a location pointed to by said memory address.